AN884

Driving Capacitive Loads With Op Amps

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INTRODUCTION

Operational amplifiers (op amps) that drive large capacitive loads tend to have peaking and oscillation problems when they are not properly compensated. Other problems include: reduced bandwidth, lower output slew rate, and higher power consumption.

This application note explains why these problems occur, how to modify the op amp circuit for better performance, and how to quickly compute circuit values.

SIMPLIFIED OP AMP MODEL

In order to understand how capacitive loads affect op amps, we must look at the op amp output impedance and bandwidth. Figure 1 shows a simplified AC model of an op amp configured for a non-inverting gain of G_N. The open-loop gain is represented by the dependent source with gain $A_{OL}(s)$, where $s = j\omega = j2\pi f$. The output stage is represented by the resistor R_O (open-loop output resistance).

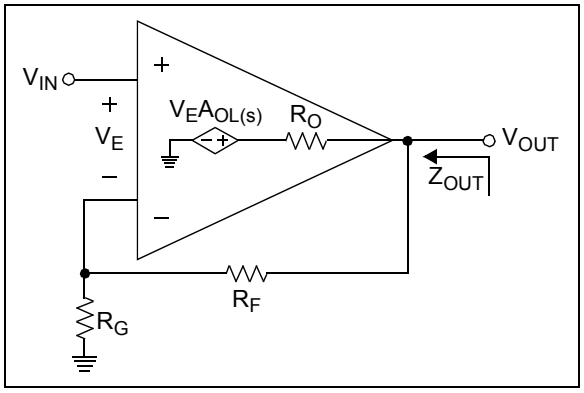

FIGURE 1: *Op amp model.*

We will include gain bandwidth product (f_{GBP}), the open-loop gain's "second pole" (f_{2P}) and the non-inverting gain (G_N) in our open-loop gain ($A_{OL}(s)$) model. Low frequency effects are left out for simplicity.

$$A_{OL}(s) \approx 1 / \left(\frac{s \cdot G_N}{\omega_{GBP}} \left(1 + \frac{s}{\omega_{2P}} \right) \right)$$

f_{2P} models the open-loop gain's reduced phase margin (PM < 90°) at high frequencies due to internal parasitics. Both f_{2P} and the capacitive load (C_L) reduce the feedback loop's phase margin.

The op amp feedback loop (R_F and R_G) causes its closed-loop behavior to be different from its open-loop behavior. Gain bandwidth product (f_{GBP}) and open-loop output impedance (R_O) are modified to give closed-loop bandwidth (f_{3dBA}) and output impedance (Z_{OUT}). We can analyze the circuit in Figure 1 to give:

$$G_N = 1 + \frac{R_F}{R_G}$$

$$f_{3dBA} \approx \frac{f_{GBP}}{G_N}$$

$$Z_{OUT} = R_O / \left(1 + \frac{A_{OL}(s)}{G_N} \right), \qquad R_F + R_G \gg R_O$$

Figure 2 shows Z_{OUT}'s behavior. At low frequencies, it is constant because the open-loop gain is constant. As the open-loop gain decreases with frequency, Z_{OUT} increases. Past f_{3dB}, the feedback loop has no more effect and Z_{OUT} stays at R_O. The peaking at G_N = +1 is caused by the reduced phase margin due to f_{2P}.

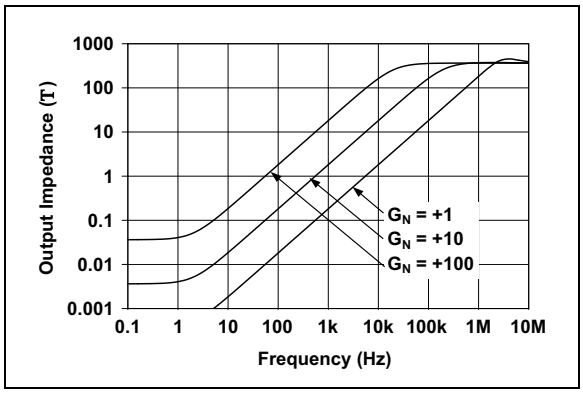

FIGURE 2: *MCP6271's Closed-Loop Output Impedance vs. Frequency.*

Figure 3 shows a simple AC model that approximates this behavior. The amplifier models the no-load gain and bandwidth, while the inductor and resistor model the output impedance vs. frequency.

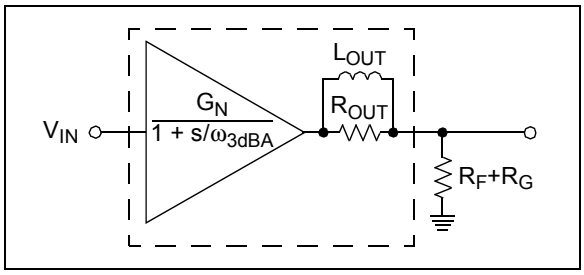

FIGURE 3: *Simplified AC model.*

The equations for L_{OUT} and R_{OUT} are:

$$L_{OUT} = G_N R_O / (2\pi f_{GBP})$$

$$R_{OUT} \approx R_O / \left(1 - \frac{f_{GBP}}{G_N f_{2P}}\right), \qquad \frac{f_{GBP}}{G_N} \le \frac{f_{2P}}{2}$$

Note that R_{OUT} is larger than R_O in order to include f_{2P}'s phase shift effects, especially at low gain (G_N).

CAPACITIVE LOAD COMPENSATION

Our discussion on compensating capacitive loads is divided into three topics. First, we will show the effect of capacitive loads when there is no compensation. Second, we will show a simple compensation method, and how it improves circuit behavior. Last, we will show how to deal with inverting circuits.

Capacitive Load

Figure 4 shows a non-inverting gain circuit with an uncompensated capacitive load. For small capacitive loads and high gains (typically C_L/G_N < 100 pF), this circuit works quite well.

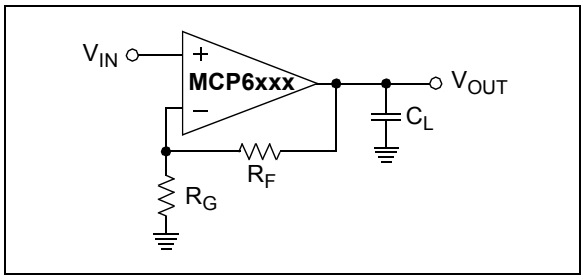

FIGURE 4: *Uncompensated capacitive load.*

Replacing the op amp in Figure 4 with the simplified op amp AC model gives a LC resonant circuit (L_{OUT} and C_L). When C_L becomes large enough, R_{OUT} does a poor job of dampening the LC resonance, which causes peaking and step response overshoot. Also, the overall closed-loop bandwidth (f_{3dB}) is reduced.

We recommend setting $R_F + R_G >> R_{OUT}$ for better circuit performance. A simplified transfer function is:

$$\frac{V_{OUT}}{V_{IN}} \approx G_N \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

where:

$$\omega_P = 2\pi f_P = 1/\sqrt{L_{OUT} C_L}$$

$$Q_P = R_{OUT} \cdot \sqrt{C_L / L_{OUT}}, \qquad R_F + R_G \gg R_{OUT}$$

Now that we have estimates of f_P and Q_P, we can use the equations in Appendix A to estimate bandwidth (f_{3dB}), frequency response peaking (H_{PK}/G_N) and step response overshoot ($\%_{ovrsht}$). Note that f_{3dB} is not the same as the op amp's no load -3dB bandwidth (f_{3dBA}).

MCP6271 Example (Uncompensated)

The equations above were used to generate the curves in Figure 5 and Figure 6 for Microchip's MCP6271 op amp. The parameters used are (see Appendix B): f_{GBP} = 2.0 MHz, f_{2P} = 4.5 MHz and R_O = 360Ω. As can be seen at G_N = =+1 V/V and C_L = 100 pF, the response peaks enough to be a concern.

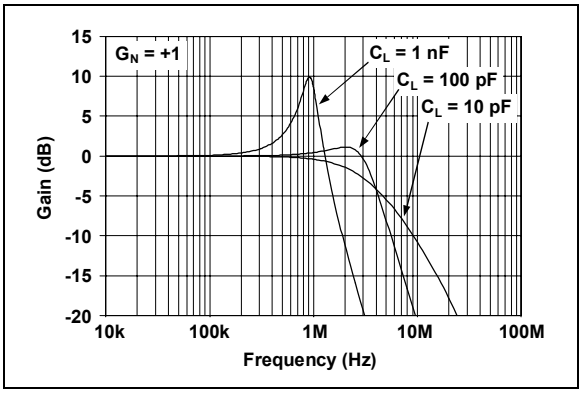

FIGURE 5: *Estimate of MCP6271's AC response with G_N = +1.*

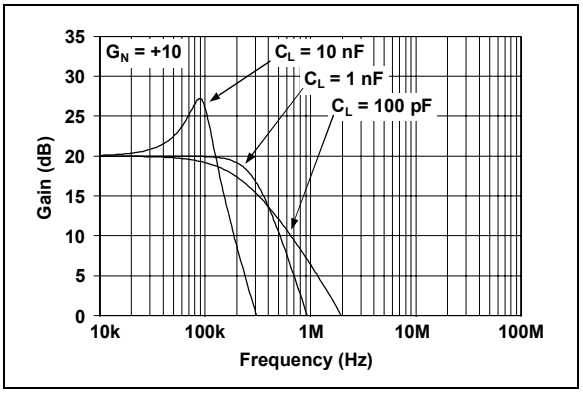

FIGURE 6: *Estimate of MCP6271's AC response with G_N = +10.*

The peaking (H_{PK}/G_N) should be near 0 dB for the best overall performance. Keeping the peaking below 3 dB usually gives enough design margin for changes in op amp, resistor and capacitor parameters over temperature and process. However, the performance is degraded.

For this example, our formulas give the estimated results shown in Table 1. As C_L increases and gain decreases, there is more peaking.

TABLE 1: RESPONSE ESTIMATES

Circuit		Response				
G_N (V/V)	C_L (F)	f_P (Hz)	Q_P ( )	f_{3dB} (Hz)	H_{PK}/G_N (dB)	$\%_{vrsht}$ (%)
1.0	10p	9.4M	0.31	3.2M	0	0
	100p	3.0M	0.98	3.7M	1.1	15
	1n	940k	3.1	1.4M	9.9	60
10.0	100p	940k	0.22	220k	0	0
	1n	300k	0.71	295k	0	4
	10n	94k	2.2	140k	7.2	49

Compensated Capacitive Load

The simplest compensation method for capacitive loads is shown in Figure 7. The resistor R_{ISO} is used to load down the LC resonant circuit, which reduces frequency response peaking. As can be seen, R_{ISO} does not change the DC response or power and only costs one additional resistor.

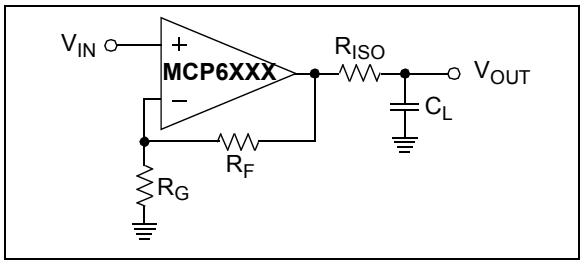

FIGURE 7: *Compensated capacitive load.*

The simplified op amp AC model produces the following transfer function, where, again, we require $R_F + R_G >> R_{OUT}$.

$$\frac{V_{OUT}}{V_{IN}} \approx G_N / \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2} \right)$$

where:

$$\omega_P = 2\pi f_P = 1/\sqrt{L_{OUT} C_L \left(1 + \frac{R_{ISO}}{R_{OUT}} \right)}$$

$$Q_P = 1/\left(\omega_P \left(\frac{L_{OUT}}{R_{OUT}} + R_{ISO} C_L \right) \right), \quad R_F + R_G » R_{OUT}$$

With these equations, we can now find a reasonable R_{ISO} value. When $Q_P = 1/\sqrt{2}$, the response has the highest possible bandwidth without peaking, and the equations are in their simplest form.

$$Q_P = 1/\sqrt{2} \approx 0.707$$

$$R_{ISO} = 0, \qquad C_L \le L_{OUT}/(2R_{OUT}^2)$$

$$R_{ISO} = \frac{L_{OUT}}{R_{OUT} C_L} \cdot \sqrt{\frac{2R_{OUT}^2 C_L}{L_{OUT}} - 1}, \qquad C_L > \frac{L_{OUT}}{2R_{OUT}^2}$$

MCP6271 Example (Compensated)

These equations were used to compensate the MCP6271 circuits represented in Figure 5 and Figure 6. The same parameters were assumed, with the only change being the addition of R_{ISO}. The improved results are shown in Figure 8 and Figure 9. Table 2 shows much better results than Table 1.

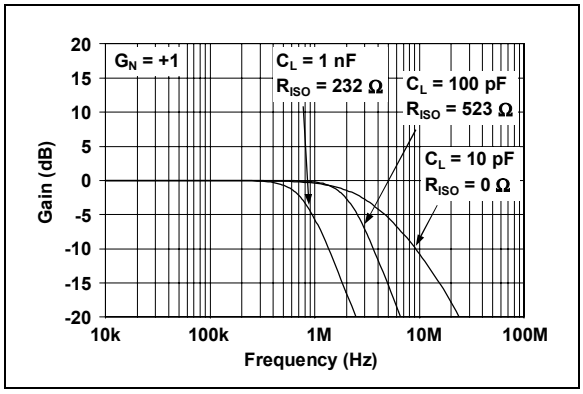

FIGURE 8: *Estimate of MCP6271's compensated AC response with G = +1.*

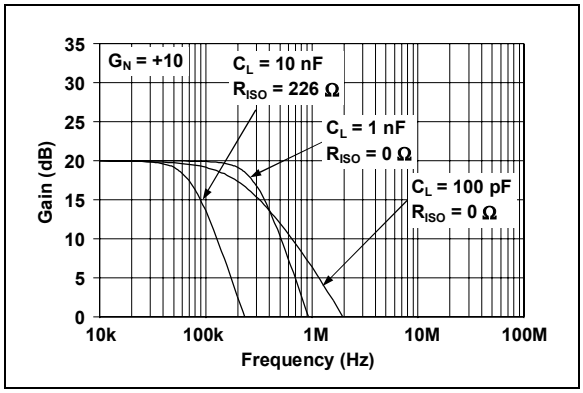

FIGURE 9: *Estimate of MCP6271's compensated AC response with G = +10.*

TABLE 2: RESPONSE ESTIMATES.

Circuit			Response				
G_N (V/V)	C_L (F)	R_{ISO} (Ω)	f_P (Hz)	Q_P ( )	f_{3dB} (Hz)	H_{PK}/G_N (dB)	$\%_{vrsht}$ (%)
1.0	10p	0	9.4M	0.31	3.2M	0	0
	100p	523	2.1M	0.71	2.1M	0	4
	1n	232	780k	0.71	780k	0	4
10.0	100p	0	940k	0.22	220k	0	0
	1n	0	300k	0.71	300k	0	4
	10n	226	74k	0.71	74k	0	4

Figure 10 shows the R_{ISO} values for the MCP6271 estimated by the above equations. It is shown versus normalized load capacitance (C_L/G_N) for ease of interpretation. Measured data for one representative part is shown in Figure 11.

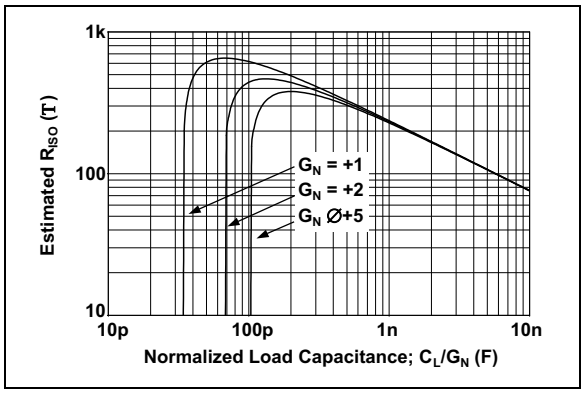

FIGURE 10: *Estimated R_{ISO} for the MCP6271.*

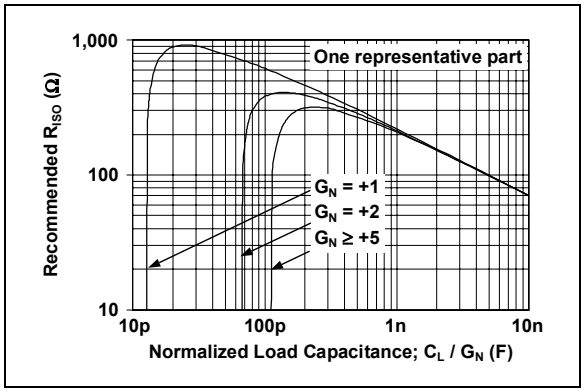

FIGURE 11: *Recommended R_{ISO} for the MCP6271.*

The main difference between Figure 10 and Figure 11 is at G_N = +1. The reduced phase margin at low G_N (caused by f_{2P}) requires additional compensation at low C_L. The simplified equations in this application note give reasonable estimates in this condition, but are not exact.

When large capacitive loads give lower op amp bandwidth than desired, refer to Microchip's line of Power MOSFET Drivers at www.microchip.com.

Inverting Gains

Inverting gain circuits (see Figure 12) are compensated in the same way as non-inverting gain circuits. Since the inverting input of the op amp is at virtual ground, the load presented to the output by the feedback network is now R_F instead of $R_F + R_G$. Thus, we need to set $R_F >> R_{OUT}$. Use the noise gain:

$$G_N = 1 + \frac{R_F}{R_G}$$

in the previous equations, even though the inverting gain is $-R_F/R_G$. For example, an inverting gain of -1 V/V gives G_N = +2. The reasons for this behavior come from op amp feedback theory [1, 3].

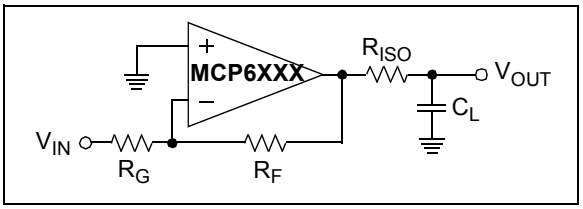

FIGURE 12: *Compensated inverting gain circuit.*

SLEW RATE

In Figure 7 and Figure 12, the op amp will produce an output current (I_{OUT}) that goes into C_L. This current cannot exceed the op amp's output short circuit current (I_{SC}). This current limit causes the output slew rate to be limited (SR_{CL}). Note that SR_{CL} is independent of the op amp's internally-set slew rate (SR). We can derive SR_{CL} as follows.

$$\frac{dV_{OUT}(t)}{dt} = \frac{I_{OUT}(t)}{C_L}$$

$$SR_{CL} = max\left(\frac{dV_{OUT}(t)}{dt}\right) = \frac{I_{SC}}{C_L}$$

where:

SR_{CL} is in units of V/s

Slew Rate and Sine Waves

Sine waves with edge rates faster than SR_{CL} or SR will cause signal distortion problems. The sine wave

$$V_{OUT}(t) = V_M sin(2\pi ft)$$

has a maximum edge rate of

$$max\left(\frac{dV_{OUT}(t)}{dt}\right) = 2\pi f V_M$$

where:

V_M is the peak output voltage

Thus, we need to keep

$$2\pi f V_M < min(SR_{CL}, SR)$$

One solution is to low-pass filter the signal before it reaches C_L. The filter bandwidth needs to satisfy

$$BW < \frac{min(SR_{CL}, SR)}{2\pi V_M}$$

Another solution is to add R_{ISO}, as shown in Figure 7 and Figure 12. The maximum current occurs when $V_{OUT}(t) = 0$; at this point the voltage across R_{ISO} is V_M. Thus, we need

$$R_{ISO} > V_M / I_{SC}, \qquad 2\pi f V_M > min(SR_{CL}, SR)$$

This choice will also reduce the signal bandwidth to meet the limit given above. The equations in the "Compensated Capacitive Load" section and Appendix A can be used to find the resulting performance as long as the signal's slew rate does not exceed SR or SR_{CL}.

When large capacitive loads cause a lower slew rate than desired, refer to Microchip's line of Power MOSFET Drivers at www.microchip.com.

Sine Wave Example

Let's look at the MCP6271 with G = +1 V/V and C_L = 1.0 µF. In Appendix B, we find SR = 0.9 V/µs and I_{SC} = 25 mA. This gives:

$$SR_{CL} = 0.028 V/\mu s$$

which is much lower than SR. With a maximum peak voltage of $2.5V_{PK}$, we need an input signal with a bandwidth less than 1.8 kHz.

If we use R_{ISO} to limit the output current, we need it to be > 100Ω. Setting R_{ISO} = 130Ω gives:

$$Q_P = 0.046$$

$$f_{3dB} = 1.2 \text{ kHz}$$

Note that if we used the R_{ISO} value for response peaking elimination (7.6Ω), we would achieve a wider bandwidth (29 kHz), but would need to keep $V_M < 0.15\ V_{PK}$ to avoid output current limiting and severe signal distortion.

Slew Rate and Square Waves

Square waves with fast edges can also cause problems with capacitive loads. The maximum edge rate of a square wave with a (10% to 90%) rise time of t_r and a peak-to-peak voltage of V_{PP}, can be approximated as:

$$max\left(\frac{dV_{OUT}(t)}{dt}\right) \approx \frac{0.8 V_{PP}}{t_r}$$

Thus, we need to keep

$$0.8 V_{PP} / t_r < min(SR_{CL}, SR)$$

One solution to this problem is to use square waves with lower edge rates (higher t_r). Filtering the square waves (lowpass filter bandwidth < $0.35/t_r$) is another approach. Using slower logic gates may be a solution in some cases. It is also possible to add R_{ISO}, as shown in Figure 7 and Figure 12. The maximum current occurs when the ideal output just reaches the new level and $V_{OUT}(t)$ is still slew rate limited. To keep $I_{OUT} < I_{SC}$, we need:

$$R_{ISO} > \frac{V_{PP} - (t_r / 0.8) min(SR_{CL}, SR)}{I_{SC}}$$

Using R_{ISO} will both slow the edges down and change the shape of the transitions.

When large capacitive loads cause a lower slew rate than desired, refer to Microchip's line of Power MOSFET Drivers at www.microchip.com.

Square Wave Example

Let's use the MCP6271 with G = +1 V/V and C_L = 100 nF. In Appendix B, we find SR = 0.9 V/µs and I_{SC} = 25 mA. We can then calculate:

$$SR_{CL} = 0.25 V/\mu s$$

which is significantly slower than SR. With a maximum voltage swing of $5.0V_{PP}$, we need an input signal with a rise time > 16 µs.

Filtering the input square wave at the input of the op amp would require a bandwidth less than 22 kHz.

If we use R_{ISO} to limit the output current, (with a maximum voltage swing of $5.0V_{PP}$ and an input rise time of 10 µs), we need R_{ISO} > 75Ω. Setting R_{ISO} = 100Ω gives:

$$Q_P = 0.18$$

$$f_{3dB} = 16 \text{ kHz}$$

Note that if we used the R_{ISO} value for response peaking elimination (24.0Ω), we would achieve a wider small signal bandwidth (92 kHz), but would need to keep $V_{PP} < 3.7V_{PP}$ to avoid output current limiting and reduced rise and fall times.

POWER DISSIPATION

It is well known that reactive elements (ideal capacitors and inductors) do not dissipate power. However, an op amp driving a reactive load will dissipate power. This happens because load current in the output stage always flows in a direction that dissipates power. The output transistors rectify the load current.

Figure 7 and Figure 12 show the circuits under discussion. There will be no DC load current because C_L blocks DC. At low frequencies, I_Q (op amp's quiescent current) and C_L will dominate the output current behavior. At high frequencies, R_{ISO} will dominate.

Given an output voltage of

$$V_{OUT}(t) = V_M sin(2\pi ft)$$

it can be shown that the average power dissipated by the op amp at low frequencies is:

$$P_{OA} = (V_{DD} - V_{SS})(I_Q + 2V_M f C_L), \qquad f \ll \frac{1}{2\pi R_{ISO} C_L}$$

The power dissipation increases with frequency because C_L dominates the load.

At high frequencies, the average power dissipated by the op amp becomes constant because R_{ISO} dominates:

$$P_{OA} = (V_{DD} - V_{SS})\left(I_Q + \frac{V_M}{\pi R_{ISO}}\right) - \frac{V_M^2}{R_{ISO}},$$

$$f \gg \frac{1}{2\pi R_{ISO} C_L}$$

In the frequency range where neither C_L or R_{ISO} dominates the load ($f \approx 1/(2\pi R_{ISO} C_L)$), a somewhat conservative estimate of P_{OA} is the minimum value from the two formulas above.

DESIGN VERIFICATION

We recommend that you always verify the performance of your circuit design with SPICE simulations and by breadboarding it on the bench. SPICE macro models of Microchip's op amps are available on the Microchip web site at www.microchip.com for your convenience.

SUMMARY

We have seen that op amps that drive large capacitive loads tend to show peaking and oscillation, reduced bandwidth, lower output slew rate, and higher power consumption. Adding one resistor to the circuit can greatly improve the performance. The resulting bandwidth is a little under the no load bandwidth.

Simple formulas were given that allow a circuit designer to quickly evaluate the impact of capacitive loads. The fix is easy to implement and understand.

Designs that need to drive large capacitors at high bandwidth or rise time may benefit from using Microchip's line of Power MOSFET Drivers.

APPENDIX A: RESPONSE MODEL

In this application note, we have seen transfer functions of the form:

$$\frac{V_{OUT}}{V_{IN}} \approx K / \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

This is a 2nd order, low-pass response, which models the op amp circuits in this application note reasonably well. We will show some simple formulas for sine wave and step responses which help evaluate the performance of the circuits in this application note [2,4].

Given f_P ($\omega_P = 2\pi f_P$) and Q_P, we can calculate the bandwidth (f_{3dB}), peak response frequency (f_{PK}) and gain peaking (H_{PK}/G_N) for a sine wave as follows:

$$f_{3dB} = \frac{f_P Q_P}{\sqrt{\frac{1}{2} - Q_P^2 + \sqrt{\left(\frac{1}{2} - Q_P^2\right)^2 + Q_P^4}}}, \qquad Q_P < 0.7$$

$$f_{3dB} = f_P \sqrt{1 - \frac{1}{2Q_P^2} + \sqrt{\left(1 - \frac{1}{2Q_P^2}\right)^2 + 1}}, \qquad Q_P \geq 0.7$$

$$f_{PK} = 0, \qquad Q_P \leq 1/\sqrt{2}$$

$$f_{PK} = f_P \sqrt{1 - \frac{1}{2Q_P^2}}, \qquad Q_P > 1/\sqrt{2}$$

$$\frac{H_{PK}}{K} = 1, \qquad Q_P \leq 1/\sqrt{2}$$

$$\frac{H_{PK}}{K} = Q_P / \sqrt{1 - \frac{1}{4Q_P^2}}, \qquad Q_P > 1/\sqrt{2}$$

The step response overshoot ($\%_{ovrsht}$) and rise time (t_r) are calculated, as follows:

$$\%_{ovrsht} = 0\%, \qquad Q_P \leq 1/2$$

$$\%_{ovrsht} = (100\%) e^{-\pi/\left(\sqrt{4Q_P^2 - 1}\right)}, \qquad Q_P > 1/2$$

$$t_r \approx 0.35 / f_{3dB}$$

It is relatively simple to extract K, f_P and Q_P from frequency response simulations or measurements.

- K is the gain at low frequencies ($f << f_{3dB}$)
- f_P is the frequency where the phase is -90°
- $|V_{OUT}/V_{IN}|$ at f_P is KQ_P (in units of V/V)

APPENDIX B: MICROCHIP OP AMPS

The performance parameters of some Microchip op amps shown in Table B-1 below are typical and were extracted from the parts' data sheets. These data sheets contain the officially-supported specifications, and can be found on Microchip's website at www.microchip.com. This data is current as of August, 2003.

TABLE B-1: TYPICAL MICROCHIP OP AMP PARAMETERS.

Part	f_{GBP} (Hz)	f_{2P} (Hz)	SR (V/µs)	R_O (Ω)	I_{SC} (mA)
MCP6041	14k	45k	0.0030	37k	21
TC1034 **(Note 1)**	60k	1.1M	0.035	15k	8
MCP6141	100k	55k	0.024	28k	21
MCP606	155k	620k	0.080	4.2k	17
MCP616	190k	1.1M	0.080	5.0k	17
MCP6001	1.0M	45M	0.6	780	23
MCP6271	2.0M	4.5M	0.9	360	25
MCP601	2.8M	20M	2.3	680	20
MCP6281	5.0M	14M	2.5	170	25
MCP6291	10M	27M	7.0	105	25
MCP6021	10M	124M	7.0	110	30

Note 1: These parameters also apply to the TC1026, TC1029, TC1030 and TC1035.

2: f_{2P} can be estimated from the Open-Loop Gain plots in the data sheet. Estimate the frequency (f_{-135}) where the Open-Loop Phase is -135° (i.e., the phase margin is 45°). Adjust for the typical capacitive load used in the measurements (C_{Ltyp}):

$$\phi_{CLtyp} \approx atan(2\pi f_{-135} R_O C_{Ltyp})$$

$$f_{2P} \approx f_{-135} / tan(45° - \phi_{CLtyp}), \qquad \phi_{CLtyp} \leq 40°$$

$$f_{2P} \approx 12 f_{-135}, \qquad \phi_{CLtyp} > 40°$$

APPENDIX C: REFERENCES

[1] Bonnie Baker, “Operational Amplifier AC Specifications and Applications,” Microchip Application Note 723 (DS00723).

[2] Charles Phillips and H. Troy Nagle, “Digital Control System Analysis and Design”, 2nd ed., Prentice Hall, 1990, pp 192-3.

[3] Adel Sedra and Kenneth Smith, Microelectronic Circuits, 3rd ed., Saunders College Publishing, 1991, Chapter 8.

[4] Benjamin Kuo, “Automatic Control Systems”, 5th ed., Prentice Hall, 1987.

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Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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